## REMARKS

The applicants consider that an interview would be helpful in the present application, and the applicants' representatives will attempt to contact the Examiner in the near future to schedule an interview. However, should the Examiner be ready to act on the present amendment before an interview has been scheduled, it is respectfully requested that the Examiner contact the undersigned attorney to schedule an interview prior to issuing another Office Action if the amendment does not place the application in condition for allowance.

The specification has been amended. Claims 1-15 are pending, with claims 1, 10, and 14-15 being independent.

Attached hereto is an Appendix entitled "Version with Markings to Show Changes Made" which is a marked-up version of the portions of the application which have been amended by the present amendment, with underlining indicating added matter.

Claims 1-15 were rejected under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 which issued from parent application Serial No. 09/043,534 of the present application. This rejection is respectfully traversed.

In explaining the rejection, the Examiner states as follows:

> The term "AND functional circuit" in the independent claims of the present application and the term "AND logical circuit" in the allowed independent claims of the prior U.S. Patent No. 6,329,973 are directed to the same AND gate circuit, therefore, claims 1-15 of the present application are claiming the

same invention as that of claims 1-9, 11-16 of prior U.S. Patent No. 6,329,973.

Claims 1-15 of the present application are respectively identical to claims 1-9 and 11-16 of U.S. Patent No. 6,329,973, except that the term AND logical circuit in the last paragraph of independent patent claims 1, 11, and 15-16 has been changed to AND functional circuit in independent application claims 1, 10, and 14-15 which respectively correspond to independent patent claims 1, 10, and 15-16.

The Examiner's position that application claims 1-15 claim the same invention as that of patent claims 1-9 and 11-16 appears to be based on the Examiner's position that the AND functional circuit recited in independent application claims 1, 10, and 14-15 and the AND logical circuit recited in independent patent claims 1, 11, and 15-16 read on AND gate circuit 47 shown, for example, in Fig. 1 and described, for example, on page 8, lines 21-22, of the specification as originally filed.

However, it is submitted that the proper test of whether application claims 1-15 claim the same invention as that of patent claims 1-9 and 11-16 is set forth in MPEP 804, Eighth Edition, August 2001, pp. 800-20 to 800-21, which provides as follows in pertinent part (emphasis added):

> ***A. Statutory Double Patenting — 35 U.S.C. 101***
>
> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. "Same invention" means identical subject matter. *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel*, 422 F.2d 438, 164 USPQ

619 (CCPA 1970); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

> A reliable test for double patenting under 35 U.S.C. 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970). Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist. For example, the invention defined by a claim reciting a compound having a "halogen" substituent is not identical to or substantively the same as a claim reciting the same compound except having a "chlorine" substituent in place of the halogen because "halogen" is broader than "chlorine." On the other hand, claims may be differently worded and still define the same invention. Thus, a claim reciting a widget having a length of "36 inches" defines the same invention as a claim reciting the same widget having a length of "3 feet."

Here, it is submitted that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 is broader than the term AND logical circuit recited in independent patent claims 1, 11, and 15-16, such that there are embodiments of the invention which fall within the scope of application claims 1-15 but do not fall within the scope of patent claims 1-9 and 11-16.

For example, it is submitted that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 means any circuit which performs an AND function, while the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 means a logical circuit which performs an AND function.

Attached hereto is a copy of H. Taub et al., Digital Integrated Electronics, 1977, p. 440 (the first page of Chapter 13, "Analog Switches", as indicated on page xiv of the table of contents), McGraw-Hill, New York, ISBN 0-07-062921-8, which states as follows in pertinent part (emphasis added):

> Digital waveforms, ideally at least, make abrupt transitions between two separated ranges of values. One range represents logic level 1 while the other range represents logic level 0. Within each range, the exact signal level is of no significance. In logical gates all inputs and outputs are digital signals.

In light of this, it is submitted that one of ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

In contrast, it is submitted that one of ordinary skill in the art would understand that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 is not limited to an implementation with a digital circuit, but means any circuit which performs an AND function, and may be implemented with either a digital circuit, or with an analog circuit, such as, for example, an operational amplifier.

Accordingly, it is submitted that an embodiment of the present invention including an analog circuit which performs an AND function would fall within the scope of independent application claims 1, 10, and 14-15 and dependent application claims 2-9 and 11-13 depending from independent application claims 1 and 10, but would arguably not fall within the scope of independent patent claims 1, 11, and 15-16 and dependent application claims 2-9 and 12-14

depending from independent patent claims 1 and 11 because, as discussed above, one of ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

Accordingly, it is submitted that claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 under the test set forth in MPEP 804, such that claims 1-15 of the present application are not subject to a double patenting rejection under 35 USC 101 over claims 1-9 and 11-16 of U.S. Patent No. 6,329,973.

Since claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 for the reasons discussed above, it is respectfully requested that the rejection of claims 1-15 under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. patent No. 6,329,973 be withdrawn.

The above arguments were also presented on pages 4-8 of the amendment of April 25, 2002. In response to these arguments, the Examiner states as follows in the Office Action of May 23, 2002 (bold and underlining is the Examiner's):

> Applicant's arguments filed 4/25/2002 have been fully considered but they are not persuasive.
>
> Applicants' remarks regarding the 101 double patenting are not persuasive. The specification only discloses an AND gate circuit 47 for performing an AND function and is implemented with a digital circuit, the specification does not disclose or include any

> analog circuit (such as an operational amplifier) which performs an AND function. Therefore, in light of the specification, both the AND logical circuit in the patented claims and the AND functional circuit in the present claims are directed to the same AND gate circuit 47, there is no any other AND functional circuit (for example, analog circuit) to perform the AND function other than the AND gate circuit 47. Therefore, the two recitations are directed to the same circuit and are of the same scope.

With respect to the Examiner's statement that

> The specification only discloses an AND gate circuit 47 for performing an AND function and is implemented with a digital circuit . . . .

it is noted that the Examiner has not identified any portion of the specification which supports her position that AND gate 47 in Fig. 1 is implemented with a digital circuit. The Examiner's attention is directed to page 8, line 19, through page 9, line 4, of the specification as amended by the preliminary amendment of October 15, 2001, which reads as follows (emphasis added):

> Each pixel is constructed by a TN liquid crystal capacitor 49, a TFT switch 48 connected to the TN liquid crystal capacitor 49, and an AND gate circuit 47 for driving the gate of the TFT switch 48. The AND gate circuit 47 and the TFT switch 48 are formed by a CMOS process of a poly-Si TFT. The other terminal of the TFT switch 48 is connected to a signal line 45 and input terminals of the AND gate circuit 47 are connected to a vertical direction gate selection line 50 and a horizontal direction gate selection line 46 in the row and column directions, respectively.

and to page 12, line 25, through page 13, line 7, of the specification which reads as follows (emphasis added):

> When an image signal is written in the display pixel, the moving image vertical direction selecting circuit 52 selects an address in the row direction and the moving

> image horizontal direction selecting circuit 44 selects an address of the moving image in the selected row. As a result, the AND gate circuit 47 of the selected display pixel is turned on and the connected TFT switch 48 is turned on.

It is not seen where anything whatsoever in these passages of the specification or elsewhere in the application supports the Examiner's position that AND gate 47 in Fig. 1 is implemented with a digital circuit.

As the applicants understand it, the Examiner's position is that the term AND functional circuit in the application claims and the term AND logical circuit in the patent claims have the same scope because they both read on AND gate circuit 47 in Fig. 2 which is the only AND circuit disclosed in the application. However, the Examiner has not cited any basis whatsoever in the statutes, rules, procedures, and decisions in support of her position, and it is submitted that the position taken by the Examiner is improper and contrary to law because the test for a statutory double patenting rejection under 35 USC 101 is not whether terms in two claims read on the same element in the disclosure as in the Examiner' position, but whether the terms in the two claims have different scopes under the literal infringement test set forth in the pertinent part of MPEP 804, Eighth Edition, August 2001, pp. 800-20 to 800-21, which is reproduced above.

For example, assume that an application discloses a circuit including a MOSFET transistor which is the only transistor disclosed in the application, and that the application issues as a patent with claims specifically reciting a MOSFET transistor. Before the application issues as a patent, a continuation

application is filed presenting claims which are identical to the claims of the patent except that the application claims recite a transistor, rather than a MOSFET transistor as recited in the patent claims.

It is submitted that the application claims reciting a transistor are broader than the patent claims reciting a MOSFET transistor because an embodiment of the invention including a bipolar junction transistor would literally infringe the application claims reciting a transistor but would not literally infringe the patent claims reciting a MOSFET transistor, such that the application claims and the patent claims would not be defining identical subject matter and statutory double patenting under 35 USC 101 would not exist between the application claims and the patent claims under the literal infringement test set forth in the pertinent part of MPEP 804, Eighth Edition, August 2001, pp. 800-20 to 800-21, which is reproduced above.

Similarly, it is submitted that the term AND functional circuit in the claims of the present application and the term AND logical circuit in claims of U.S. Patent No. 6,329,973 do in fact have different scopes for the reasons discussed in detail above, i.e. because an embodiment of the present invention including an analog circuit which performs an AND function would fall within the scope of independent application claims 1, 10, and 14-15 and dependent application claims 2-9 and 11-13 depending from independent application claims 1 and 10, but would arguably not fall within the scope of independent patent claims 1, 11, and 15-16 and dependent application claims 2-9 and 12-14 depending from independent patent claims 1 and 11 because, as discussed above, one of

ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

Accordingly, it is submitted that claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 under the literal infringement test set forth in MPEP 804, such that claims 1-15 of the present application are not subject to a double patenting rejection under 35 USC 101 over claims 1-9 and 11-16 of U.S. Patent No. 6,329,973.

Since claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 for the reasons discussed above, it is respectfully requested that the rejection of claims 1-15 under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. patent No. 6,329,973 be withdrawn.

It is submitted that the Examiner's only rejection has been overcome, and that the application is now in condition for allowance. Entry of this amendment, reconsideration of the application, and an action of a favorable nature are respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any

overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (520.36114CX1).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Richard Schwaab Reg No 32,173 for
Melvin Kraus
Registration No. 22,466

MK/RSS
(703) 312-6600

Attachments

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Changes made to the application by the present amendment are indicated below, with underlining indicating added matter.

IN THE SPECIFICATION

The replacement section entitled "CROSS-REFERENCES TO RELATED APPLICATIONS" which was added on page 1 between line 2 ("IMAGE DISPLAY") and line 3 ("BACKGROUND OF THE INVENTION") in the amendment of April 25, 2002, has been deleted and replaced with the following replacement section:

--CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of application Serial No. 09/043,534 filed on March 20, 1998, now U.S. Patent No. 6,329,973, which is a national stage application under 35 USC 371 of international application No. PCT/JP95/01886 filed on September 20, 1995. The contents of application Serial No. 09/043,534 are hereby incorporated herein by reference in their entirety.--

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# Digital Integrated Electronics

This book was set in Times Roman.
The editors were Peter D. Nalle and Madelaine Eichberg;
the cover was designed by Scott Chelius;
the production supervisor was Charles Hess.
The drawings were done by J & R Services, Inc.
Kingsport Press, Inc., was printer and binder.

Library of Congress Cataloging in Publication Data

Taub, Herbert, date
Digital integrated electronics.

(McGraw-Hill electrical and electronic engineering series)
Includes index.
1. Digital electronics. 2. Integrated circuits.
I. Schilling, Donald L., joint author. II. Title.
TK7868.D5T37 621.381 76-4585
ISBN 0-07-062921-8

DIGITAL
INTEGRATED
ELECTRONICS



1234567890KPKP7832109876

# 13

# ANALOG SWITCHES

Digital waveforms, ideally at least, make abrupt transitions between two separated ranges of values. One range represents logic level 1 while the other range represents logic level 0. Within each range, the exact signal level is of no significance. In logical gates all inputs and outputs are digital signals.

Analog voltages, on the other hand, are voltages whose precise value is always significant. Such analog voltages may be fixed in value or may make excursions through a continuous range of values. There frequently occurs a need for switches in circuits and systems involving analog signals, in which the opening and closing of the switches are to be controlled by digital waveforms. Circuits of this type are variously called *analog gates*, *transmission gates*, *linear gates*, *time-selection circuits*, etc., depending on the purpose to which the circuit is put. The switch-control digital waveform is referred to as the *gating signal*, the *control signal*, or the *logic input*.